

# MBR20H100CTG, MBRB20H100CTG, MBRF20H100CTG, NRVBB20H100CTT4G



ON Semiconductor®

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## Switch-mode Power Rectifier 100 V, 20 A

### Features and Benefits

- Low Forward Voltage: 0.64 V @ 125°C
- Low Power Loss/High Efficiency
- High Surge Capacity
- 175°C Operating Junction Temperature
- 20 A Total (10 A Per Diode Leg)
- Guard-Ring for Stress Protection
- NRVBB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

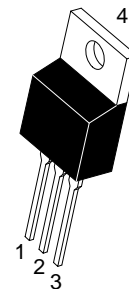
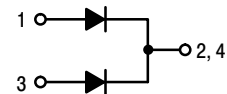
### Applications

- Power Supply – Output Rectification
- Power Management
- Instrumentation

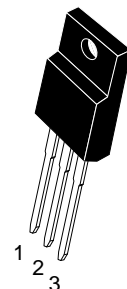
### Mechanical Characteristics:

- Case: Epoxy, Molded
- Epoxy Meets UL 94 V-0 @ 0.125 in
- Weight (Approximately):  
1.9 Grams (TO-220)  
1.7 Grams (D<sup>2</sup>PAK)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes:  
260°C Max. for 10 Seconds

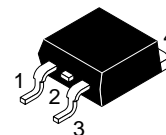
## SCHOTTKY BARRIER RECTIFIER 20 AMPERES, 100 VOLTS



TO-220  
CASE 221A  
STYLE 6



TO-220 FULLPAK™  
CASE 221D  
STYLE 3



D<sup>2</sup>PAK 3  
CASE 418B  
STYLE 3

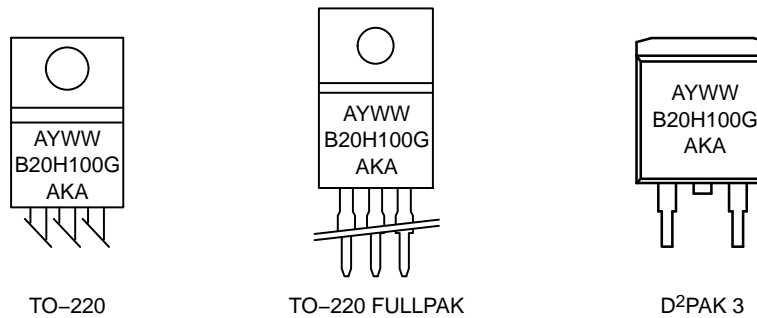
### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 2 of this data sheet.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MBR20H100CTG, MBRB20H100CTG, MBRF20H100CTG, NRVBB20H100CTT4G



A = Assembly Location  
 Y = Year  
 WW = Work Week  
 B20H100 = Device Code  
 G = Pb-Free Device  
 AKA = Polarity Designator

**Figure 1. Marking Diagrams**

## MAXIMUM RATINGS (Per Diode Leg)

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage'	$V_{RRM}$ $V_{RWM}$ $V_R$	100	V
Average Rectified Forward Current (Rated $V_R$ , $T_C = 162^\circ\text{C}$ )	$I_{F(AV)}$	10	A
Peak Repetitive Forward Current (Rated $V_R$ , Square Wave, 20 kHz) $T_C = 160^\circ\text{C}$	$I_{FRM}$	20	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	$I_{FSM}$	250	A
Operating Junction Temperature (Note 1)	$T_J$	+175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$
Voltage Rate of Change (Rated $V_R$ )	dv/dt	10,000	V/ $\mu\text{s}$
Controlled Avalanche Energy (see test conditions in Figures 11 and 12)	$W_{AVAIL}$	200	mJ
ESD Ratings: Machine Model = C Human Body Model = 3B		> 400 > 8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The heat generated must be less than the thermal conductivity from Junction-to-Ambient:  $dP_D/dT_J < 1/R_{\theta JA}$ .

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Thermal Resistance (MBR20H100CTG, MBRB20H100CTG and NRVBB20H100CTT4G)			$^\circ\text{C}/\text{W}$
Junction-to-Case	$R_{\theta JC}$	2.0	
Junction-to-Ambient (MBRF20H100CTG)	$R_{\theta JA}$	60	
Junction-to-Case	$R_{\theta JC}$	2.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MBR20H100CTG, MBRB20H100CTG, MBRF20H100CTG, NRVBB20H100CTT4G

## ELECTRICAL CHARACTERISTICS (Per Diode Leg)

Characteristic	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage (Note 2) ( $I_F = 10\text{ A}$ , $T_C = 25^\circ\text{C}$ ) ( $I_F = 10\text{ A}$ , $T_C = 125^\circ\text{C}$ ) ( $I_F = 20\text{ A}$ , $T_C = 25^\circ\text{C}$ ) ( $I_F = 20\text{ A}$ , $T_C = 125^\circ\text{C}$ )	$V_F$	0.77 0.64 0.88 0.73	V
Maximum Instantaneous Reverse Current (Note 2) (Rated DC Voltage, $T_C = 125^\circ\text{C}$ ) (Rated DC Voltage, $T_C = 25^\circ\text{C}$ )	$i_R$	6.0 0.0045	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

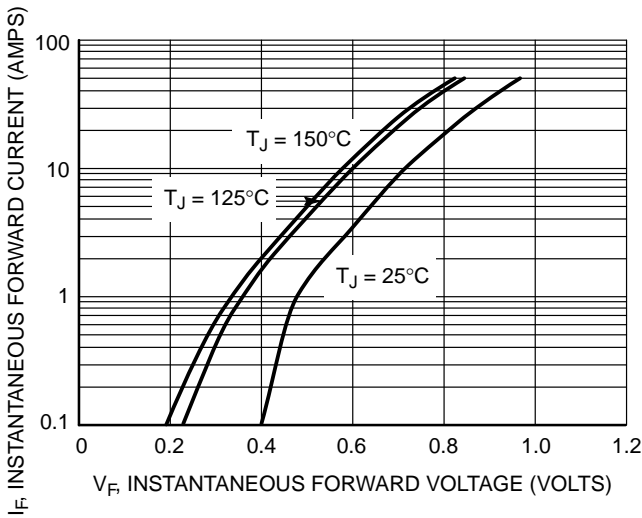
## ORDERING INFORMATION

Device Order Number	Package	Shipping <sup>†</sup>
MBR20H100CTG	TO-220 (Pb-Free)	50 Units / Rail
MBRF20H100CTG	TO-220FP (Pb-Free)	50 Units / Rail
MBRB20H100CTT4G	D <sup>2</sup> PAK 3 (Pb-Free)	800 / Tape & Reel
NRVBB20H100CTT4G*	D <sup>2</sup> PAK 3 (Pb-Free)	800 / Tape & Reel

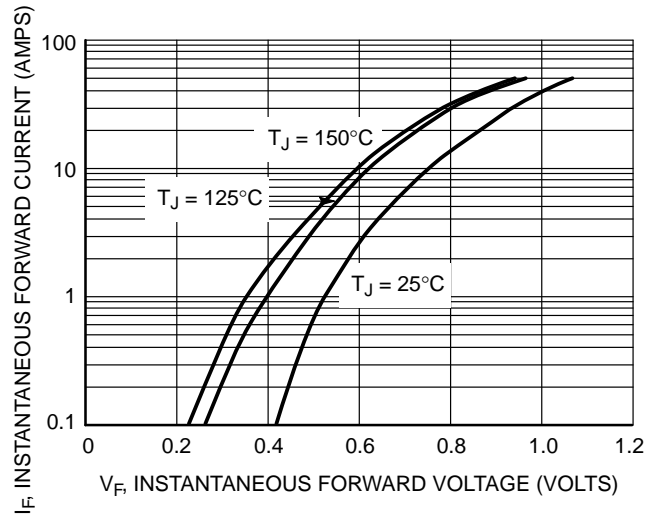
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

\*NRVBB Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

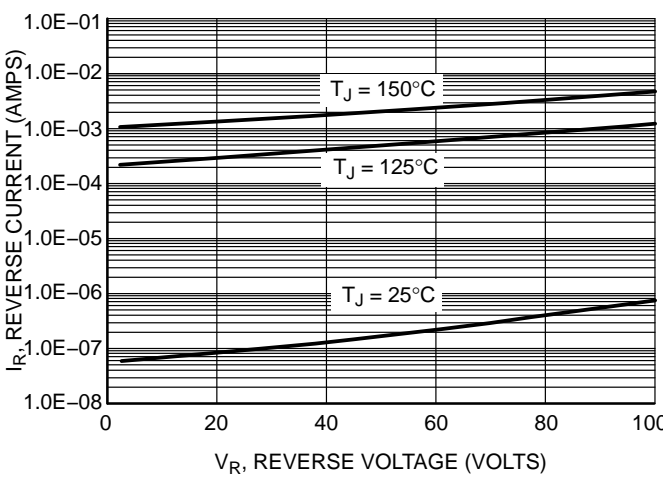
**MBR20H100CTG, MBRB20H100CTG, MBRF20H100CTG, NRVBB20H100CTT4G**



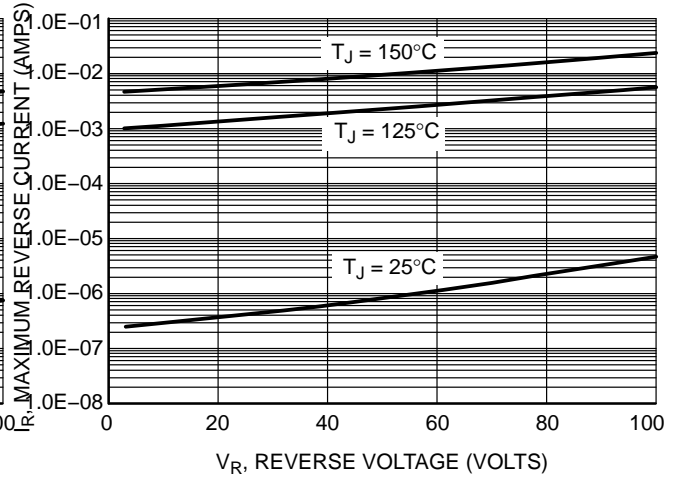
**Figure 1. Typical Forward Voltage**



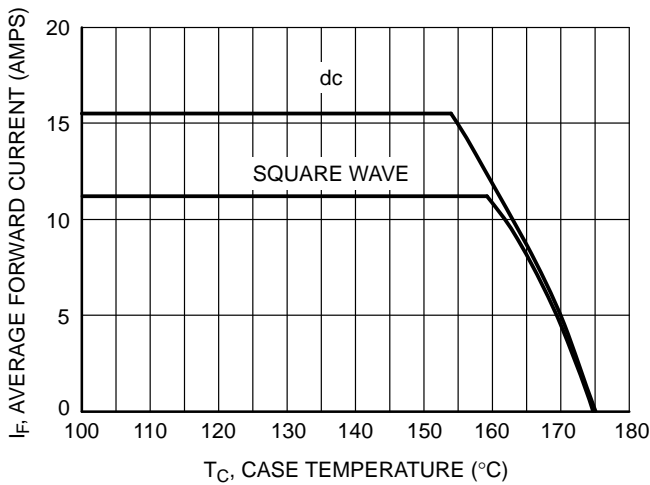
**Figure 2. Maximum Forward Voltage**



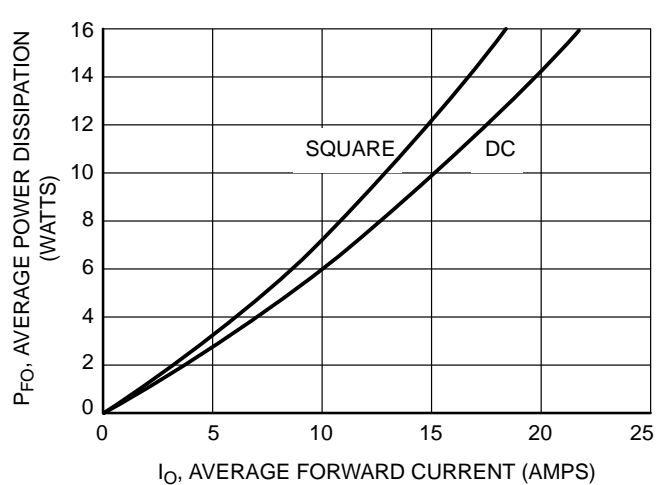
**Figure 3. Typical Reverse Current**



**Figure 4. Maximum Reverse Current**

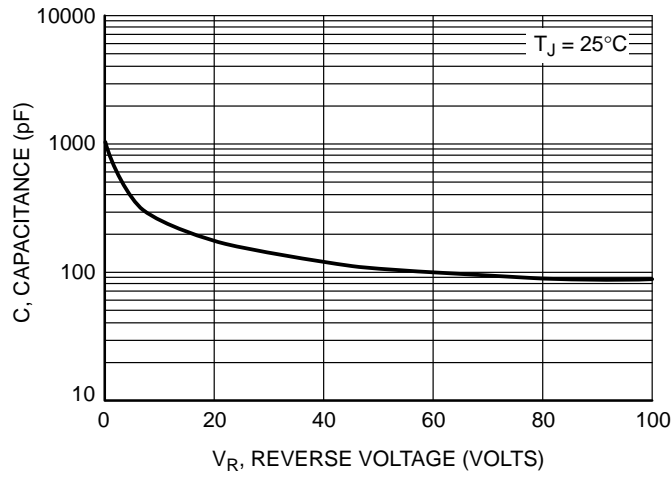


**Figure 5. Current Derating**

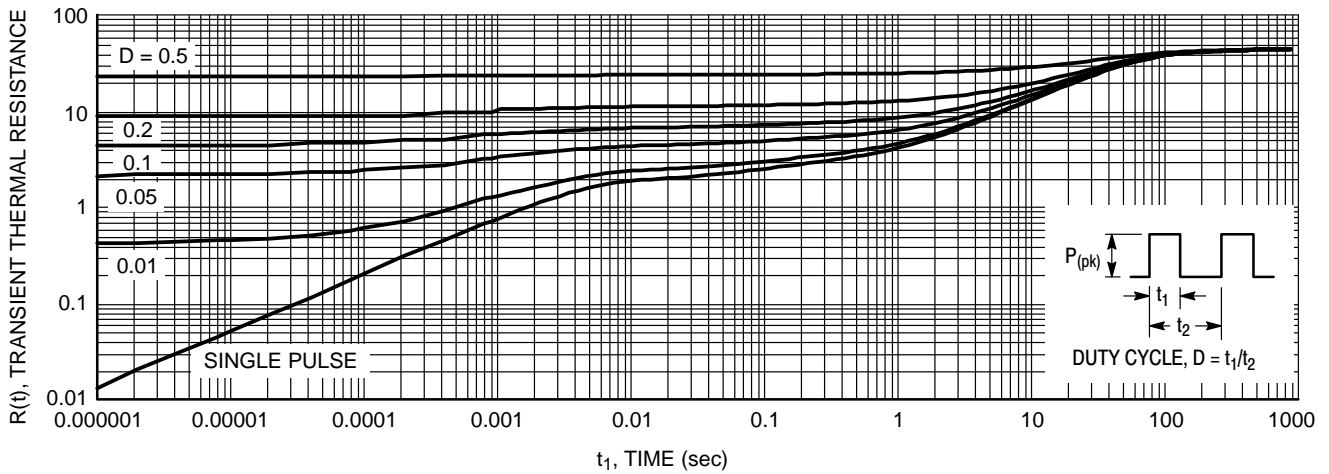


**Figure 6. Forward Power Dissipation**

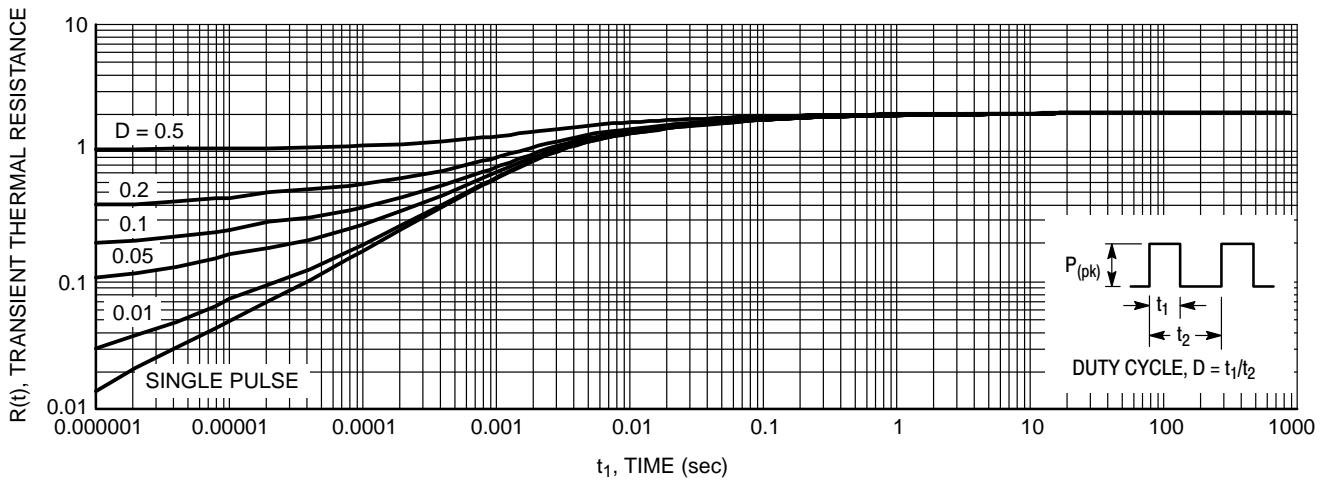
**MBR20H100CTG, MBRB20H100CTG, MBRF20H100CTG, NRVBB20H100CTT4G**



**Figure 7. Capacitance**



**Figure 8. Thermal Response Junction-to-Ambient for MBR20H100CT, MBRB20H100CT and NRVBB20H100CTT4G**



**Figure 9. Thermal Response Junction-to-Case for MBR20H100CT, MBRB20H100CT and NRVBB20H100CTT4G**

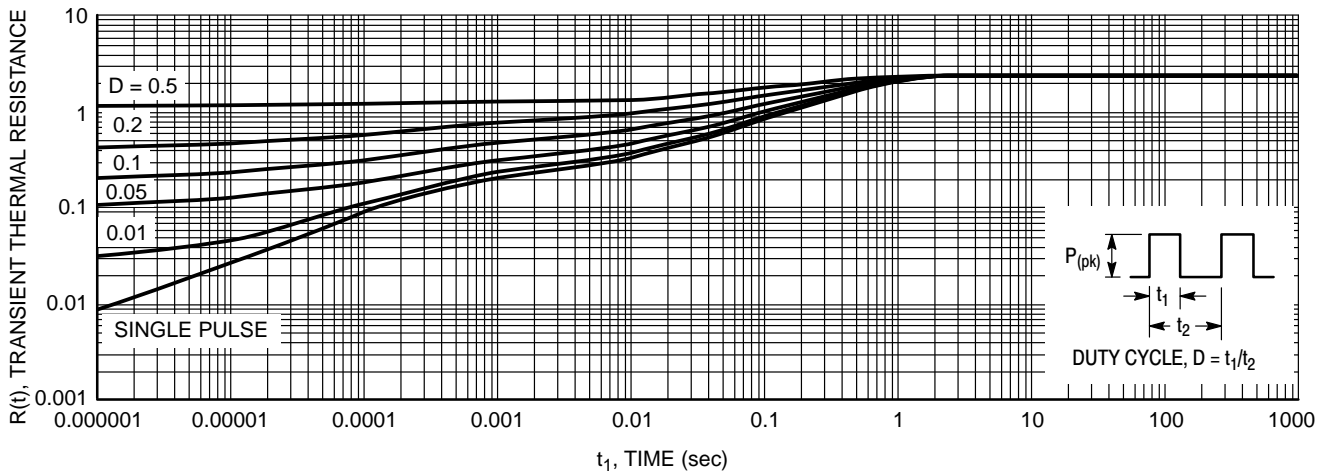


Figure 10. Thermal Response Junction-to-Case for MBRF20H100CT

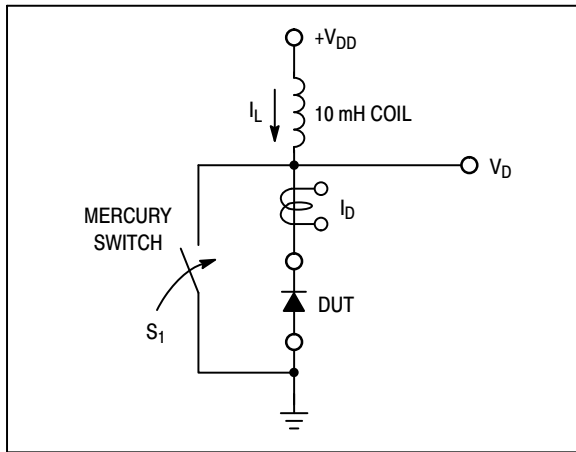


Figure 11. Test Circuit

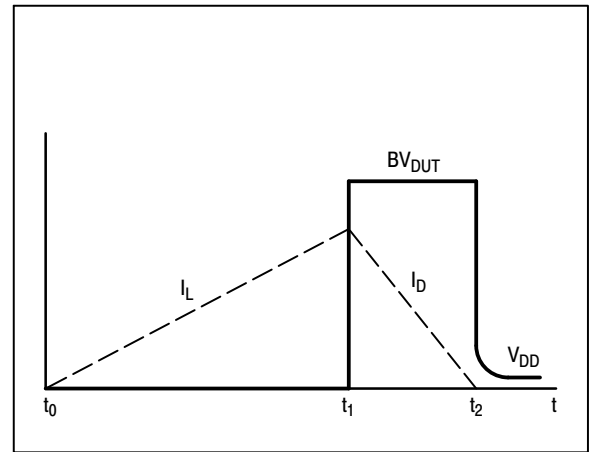


Figure 12. Current-Voltage Waveforms

The unclamped inductive switching circuit shown in Figure 11 was used to demonstrate the controlled avalanche capability of this device. A mercury switch was used instead of an electronic switch to simulate a noisy environment when the switch was being opened.

When  $S_1$  is closed at  $t_0$  the current in the inductor  $I_L$  ramps up linearly; and energy is stored in the coil. At  $t_1$  the switch is opened and the voltage across the diode under test begins to rise rapidly, due to  $di/dt$  effects, when this induced voltage reaches the breakdown voltage of the diode, it is clamped at  $BV_{DUT}$  and the diode begins to conduct the full load current which now starts to decay linearly through the diode, and goes to zero at  $t_2$ .

By solving the loop equation at the point in time when  $S_1$  is opened; and calculating the energy that is transferred to the diode it can be shown that the total energy transferred is equal to the energy stored in the inductor plus a finite amount of energy from the  $V_{DD}$  power supply while the diode is in breakdown (from  $t_1$  to  $t_2$ ) minus any losses due to finite component resistances. Assuming the component resistive

elements are small Equation (1) approximates the total energy transferred to the diode. It can be seen from this equation that if the  $V_{DD}$  voltage is low compared to the breakdown voltage of the device, the amount of energy contributed by the supply during breakdown is small and the total energy can be assumed to be nearly equal to the energy stored in the coil during the time when  $S_1$  was closed, Equation (2).

EQUATION (1):

$$W_{AVAL} \approx \frac{1}{2} L I_{LPK}^2 \left( \frac{BV_{DUT}}{BV_{DUT} + V_{DD}} \right)$$

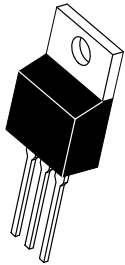
EQUATION (2):

$$W_{AVAL} \approx \frac{1}{2} L I_{LPK}^2$$

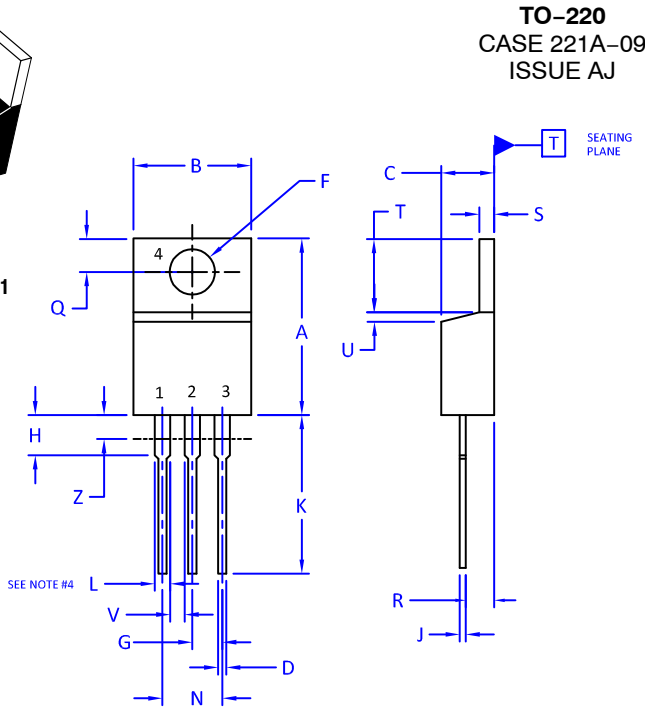
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



TO-220  
CASE 221A-09  
ISSUE AJ

DATE 05 NOV 2019

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

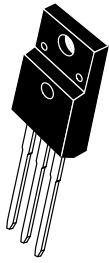
- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

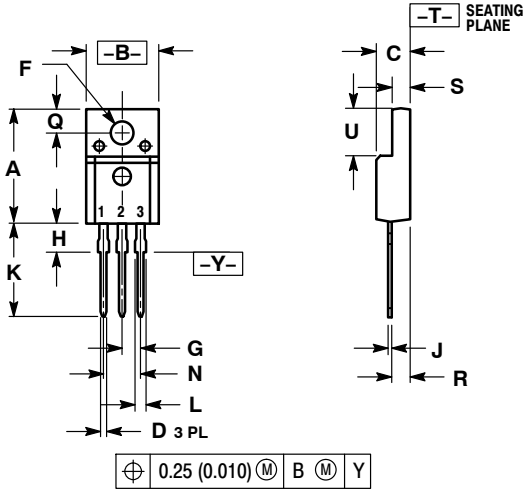
ON Semiconductor®



SCALE 1:1

## TO-220 FULLPAK CASE 221D-03 ISSUE K

DATE 27 FEB 2009



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH
  - 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

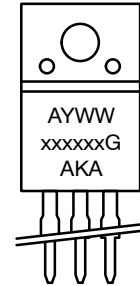
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

### MARKING DIAGRAMS

- |  |   |  |
|--|---|--|
| STYLE 1:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE     | STYLE 2:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER | STYLE 3:<br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE |
| STYLE 4:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE | STYLE 5:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE     | STYLE 6:<br>PIN 1. MT 1<br>2. MT 2<br>3. GATE      |



**Bipolar**



**Rectifier**

- |                               |                           |
|-------------------------------|---------------------------|
| xxxxxx = Specific Device Code | A = Assembly Location     |
| G = Pb-Free Package           | Y = Year                  |
| A = Assembly Location         | WW = Work Week            |
| Y = Year                      | xxxxxx = Device Code      |
| WW = Work Week                | G = Pb-Free Package       |
|                               | AKA = Polarity Designator |

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<b>DESCRIPTION:</b>	<b>TO-220 FULLPAK</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

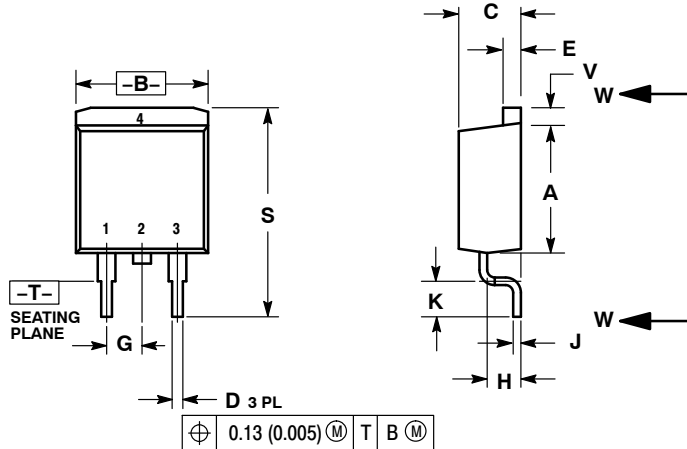
ON Semiconductor®



**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

SCALE 1:1

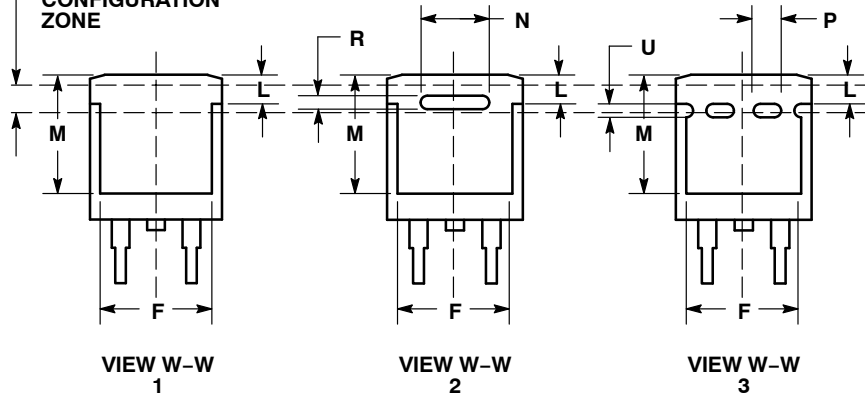


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

**VARIABLE CONFIGURATION ZONE**



- |  |   |   |  |   |  |
|--|---|---|--|---|--|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN | <b>STYLE 3:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. ANODE<br>4. CATHODE | <b>STYLE 4:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 5:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE<br>4. ANODE | <b>STYLE 6:</b><br>PIN 1. NO CONNECT<br>2. CATHODE<br>3. ANODE<br>4. CATHODE |
|--|---|---|--|---|--|

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

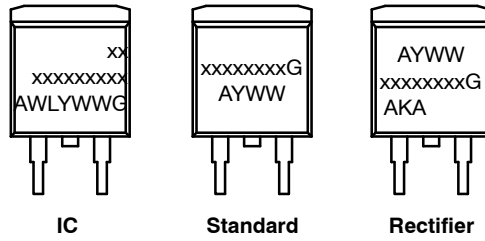
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<b>DESCRIPTION:</b>	<b>D<sup>2</sup>PAK 3</b>	<b>PAGE 1 OF 2</b>

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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

DATE 17 FEB 2015

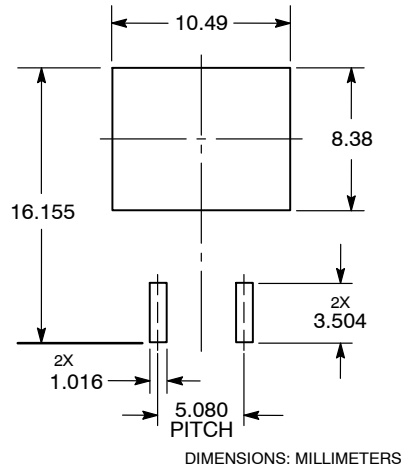
**GENERIC  
MARKING DIAGRAM\***



- xx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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